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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,614	07/21/2000	Yasuyuki Morishita	040373/0287	4521

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/621,614	MORISHITA, YASUYUKI
	Examiner	Art Unit
	Ori Nadav	2811

AK

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 and 3-11 are objected to because of the following informalities: claims 1, 4, 8 and 11 recite the limitation "said source extension region" and "said source and drain extension regions in lines 23 and 25, respectively. There is insufficient antecedent basis for this limitation in the claim.

. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Duvvury (5,502,317), Watt (5,701,024) and Van Roozendaal et al. (5,281,841).

APA teaches in figure 7 a semiconductor device having, on a semiconductor substrate 20, an input/output protection circuit section comprising a complementary N type field effect transistor wherein the complementary field effect transistor includes a first field

effect transistor having source 3c and drain 3b diffusion layers of the first conductive type, respectively, and a gate electrode 6 that is disposed between these source and drain diffusion layers of the first conductivity type, and a second field effect transistor having source 4c and drain 4b diffusion layers of the second conductive type, respectively, and a gate electrode 5 that is disposed between these source and drain diffusion layers of the second conductivity type, wherein a source dopant diffusion region 4a of the second conductive type is set at a distance from the first field effect transistor, and a drain dopant diffusion region 3a of the first conductive type is set at a distance from the second field effect transistor,

an element isolation film 10 located in the substrate between the dopant diffusion region and the source diffusion layer of the first conductivity type for separating the dopant diffusion region from the source diffusion layer,

wherein the drain dopant diffusion region 4a is connected to a first reference potential Vss, the drain dopant diffusion region 3a is connected to a second reference potential Vdd, and the drain diffusion layer 3b and the drain diffusion layer 4b of the first and second field effect transistors, respectively, are each connected directly to an input/output terminal section 7 without an intervening resistance element, and wherein the source diffusion layer of the first field effect transistor is connected to a constant ground terminal 9 and not connected to an input/output terminal section..

APA does not teach a first conductive type well formed directly under the first source diffusion layer and thereby the first conductive type well is electrically connected directly

with the source diffusion laver, and at least partially underlies the element isolation film, and having a lower dopant concentration than the first diffusion layer, and

said source and drain diffusion layers each have an extension region extending into said channel region and not extending between said source and drain diffusion layers of said first conductive type well, said extension regions having a dopant concentration between the dopant concentration of said source and drain diffusion layers and the dopant concentration of said first conductive type well.

Duvvury teach in figures 6 (or figure 9) and related text a first conductive type well 22 (or 142) formed directly under the first source diffusion layer 12 (or 114) and thereby the first conductive type well is electrically connected directly with the source diffusion laver, wherein the first conductive type well at least partially underlies the element isolation film 28 (or 128), and having a lower dopant concentration than the first diffusion layer.
Van Roozendaal et al. teach the advantages of forming a first conductive type well directly under the first source diffusion layer (column 8, lines 60-65).
Watt teaches in figure 6 source and drain diffusion layers each have extension regions 62 formed in said channel region and not extending between said source and drain diffusion layers.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer, as taught by Duvvury, and to form LDD (extension regions) in said channel region and not extending between

said source and drain diffusion layers in APA's device in order to prevent spiking and to provide better electrical isolation to the device by forming the transistor in an n-well, and in order to improve the device characteristics by using conventional LDD regions, respectively. The combination is motivated by the teachings of Van Roozendaal et al. who point out the advantages of forming a first conductive type well directly under the first source diffusion layer (column 8, lines 60-65).

Regarding the claimed limitations of forming said extension regions having a dopant concentration between the dopant concentration of said source and drain diffusion layers and the dopant concentration of said first conductive type well, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form said extension regions having a dopant concentration between the dopant concentration of said source and drain diffusion layers and said first conductive type well in APA's device in order to optimize the device characteristics. Note that generally, differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 1, APA teaches in figures 14-15 and related text that an input/output protection circuit generally composed of a plurality of field effect transistors connected in parallel, each of which has source and drain diffusion layers of the first conductive type.

Regarding claims 5, 6 and 11, APA teaches a gate electrode of the first field effect transistor and the source dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom of the first conductive type well at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well in APA's device in order to prevent shorting the junction by allowing spikes to propagate longer distance.

Regarding claim 6, APA teaches a dopant high-concentration region 20 beneath the second conductive type well, and containing second conductive type dopants with a higher dopant concentration than the second conductive type well.

Response to Arguments

Applicant argues that the advantages of using extension regions in the protective circuit structure recited in applicant's claims are not appreciated nor taught by the prior art, and prior art does not supply motivation to combine the references.

Even if applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art, this cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). The advantages of forming LDD (extension regions) regions in a semiconductor device are well known in the art. It is even conventional to use LDD regions in order to improve the device characteristics. Furthermore, Van Roozendaal et al. provide motivation to combine the references.

Note that the broad recitation of the claims does not require the first conductive type well to terminate under the element isolation film, wherein the element isolation film is in direct contact with the source region.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
7/5/05

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